

Abstract of the Disclosure

In a method for forming short-channel transistors, the method comprising the steps of: forming a first oxide layer and
5 a sacrificial layer one after another on a semiconductor substrate and etching the sacrificial layer, thus forming a residual sacrificial layer pattern; conducting an ion implantation using the residual sacrificial layer pattern as a mask, thus forming an LDD ion-implant layer in the
10 semiconductor substrate; forming the first spacers on both side walls of the residual sacrificial layer pattern; conducting an ion implantation using the residual sacrificial layer pattern and the first spacers as a mask, thus forming a source/drain ion-implant layer under the LDD ion-implant layer; forming a
15 nitride layer and a second oxide layer one after another on the whole surface of the former resultant object and conducting an annealing treatment, thus forming source/drain regions; conducting chemical-mechanical polishing (CMP) processes to the extent that an upper surface of the residual sacrificial layer
20 pattern is exposed, and removing the residual sacrificial layer pattern through etching; forming the second spacers on side walls of a portion where the residual sacrificial layer pattern is removed; conducting an ion implantation on the substrate

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between the second spacers, thus forming a punch-stop ion
implant layer; etching the first oxide layer under the portion
where the residual sacrificial layer pattern is removed, and
forming a gate insulation layer; and forming a gate on the
5 portion where the residual sacrificial layer pattern is removed.